B.TECH Vth SEMESTER
ANTENNA AND WAVE PROPAGATION
(ECE-301E)

L	T	P			
3	2	-	Theory	:	100
			Sessional	:	50
			Time	:	3Hrs

UNIT – I

BASIC PRINCIPLES AND DEFINITIONS: Retarded vector and scalar potentials. Radiation and induction fields. Radiation from elementary dipole (Hertzian dipole, short dipole, Linear current distribution), half wave dipole, Antenna parameters : Radiation resistance, Radiation pattern, Beam width, Gain, Directivity, Effective height, Effective aperture, Bandwidth and Antenna Temperature.

UNIT – II

RADIATING WIRE STRUCTURES AND ANTENNA ARRAYS: Folded dipole , Monopole, Biconical Antenna, Loop Antenna, Helical Antenna. Principle of pattern multiplication, Broadside arrays, Endfire arrays, Array pattern synthesis, Uniform Array, Binomial Array, Chebyshev Array, Antennas for receiving and transmitting TV Signals e.g. Yagi-Uda and Turnstile Antennas.

UNIT – III

APERTURE TYPE ANTENNAS: Radiation from rectangular aperture, E-plane Horns, H-plane Horns, Pyramidal Horn, Lens Antenna, Reflector Antennas .

BROADBAND AND FREQUENCY INDEPENDENT ANTENNAS : Broadband Antennas. The frequency independent concept : Rumsey's principle, Frequency independent planar log spiral antenna, Frequency independent conical spiral antenna and Log periodic antenna.

UNIT – IV

PROPAGATION OF RADIO WAVES : Different modes of propagation, Ground waves, Space waves, Surface waves and Tropospheric waves, Ionosphere, Wave propagation in the ionosphere, critical frequency, Maximum Usable Frequency (MUF), Skip distance, Virtual height, Radio noise of terrestrial and extra terrestrial origin. Multipath fading of radio waves.

NOTE

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. Robert E.Collin, Antenna & Wave Propagation, McGraw Hill
2. John D. Kraus, Antennas, McGraw Hill.
3. E.C.Jordan and K.G.Balmain, Electromagnetic Waves and Radiating Systems, PHI

B.TECH Vth SEMESTER
COMPUTER HARDWARE DESIGN
(ECE-303E)

L	T	P			
3	1	-	Theory	:	100
			Sessional	:	50
			Time	:	3Hrs

UNIT-I

BASIC STRUCTURE OF COMPUTER HARDWARE AND SOFTWARE :
Functional Units, historical Perspective, Register transfer and micro-operations. Information representation, Instruction format, Instruction types, Addressing modes, Machine and Assembly Language programming, Macros and Subroutines.

UNIT-II

PROCESSOR DESIGN: Fixed – point and floating-point arithmetic addition, subtraction, Multiplication and division, Decimal arithmetic unit – BCD adder, BCD subtraction, decimal arithmetic operations, ALU design, Forms of Parallel processing classification of Parallel structures, Array Processors, Structure of general purpose Multiprocessors.
CONTROL DESIGN:
Hardwired Control: design methods, Multiplier Control Unit, CPU Control unit, Microprogrammed Control: basic concepts, Multiplier Control Unit, Microprogrammed Computers, CPU Control unit.

UNIT-III

MEMORY ORGANIZATION: Memory device characteristics, Random access memories: semiconductor RAMS, Serial – access Memories – Memory organization, Magnetic disk memories, Magnetic tape memories, Optical memories, Virtual memory, Main Memory Allocation, Interleaved memory, Cache Memory, Associative Memory.

UNIT-IV

SYSTEM ORGANIZATION: Input-Output Systems – Programmed IO, DMA and Interrupts, IO Processors, Interconnection networks – single bus, crossbar networks, multistage networks, hypercube networks, mesh networks, Tree networks, ring networks, Pipelining – basic concept.

NOTE

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. J.P.Hayes, Computer Architecture and Organization, Mc Graw Hill.
2. M.M. Mano , Computer System Architecture, PHI.
1. V.C.Hamacher, Z.G.Vianesic & S.G.Zaky, Computer Organization , Mc-Graw Hill.

B.TECH Vth SEMESTER
INFORMATION THEORY AND CODING
(ECE-305E)

L	T	P		
4	1	-	Theory :	100
			Sessional :	50
			Time :	3 hrs.

UNIT – I

PROBABILITY AND RANDOM PROCESSES : Probability, random variables, Probability distribution and density functions, Joint Statistics, Conditional Statistics, independence, Functions of random variables & random vectors, Expectation, moments, Characteristic Functions, Convergence of a sequence of random variables, Central Limit Theorem, Random Processes, mean and Auto Correlation, Stationary ergodicity, Power Spectral density, Response of memory- less and linear systems, Gaussian Poisson, Markov processes.

UNIT – II

ELEMENTS OF INFORMATION THEORY AND SOURCE CODING: Introduction, information as a measure of uncertainty, Entropy, its properties, Discrete memoryless channels, Mutual information, its properties, BSC, BEC. Channel capacity, Shanon's theorem on coding for memoryless noisy channels. Separable binary codes, Shanon–Fano encoding, Noiseless coding, Theorem of decodability, Average length of encoded message, Shanon's binary encoding, Fundamental theorem of discrete noiseless coding, Huffman's minimum redundancy codes.

UNIT – III

LINEAR BLOCK CODES: Introduction to error control coding, Types of codes, Maximum Likelihood decoding, Types of errors and error control strategies, Galois fields, Linear block codes, Error detecting and correcting capabilities of a block code, Hamming code, cyclic code, B.C.H. codes.

UNIT – IV

CONVOLUTIONAL CODES AND ARQ: Transfer function of a convolutional code, Syndrom decoding, Majority logic decodable codes, Viterbi decoding, distance properties of binary convolutional codes, Burst error correcting convolutional codes, general description of basic ARQ strategies, Hybrid ARQ schemes.

NOTE

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. Papoulis, A. Probability, Random Variables and Stochastic Processes, MGH.
2. Gray, R.M. Davission,L.D,Introduction to Statistical Signal Processing- Web Edition-1999.
3. F. M. Reza, Information Theory, McGraw Hill.
4. Das, Mullick and Chatterjee, Digital Communication, Wiley Eastern Ltd.
5. Shu Lin and J. Costello, Error Control Coding, Prentice Hall.
6. B. R. Bhat, Modern Probability Theory, New Age International Ltd.

B.TECH Vth SEMESTER
LINEAR IC APPLICATIONS
(ECE-307E)

L	T	P
3	2	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT-I
DIFFERENTIAL AND CASCADE AMPLIFIERS: Balanced, unbalanced output differential amplifiers, FET differential amplifier, current mirrors, level Translators, cascade configuration of amplifiers, operational amplifiers, Introduction to ideal OP-AMP, characteristic parameters, Practical OP-AMP, its equivalent circuit and op-amp circuit configurations.

UNIT-II
OP-AMP WITH NEGATIVE FEEDBACK AND FREQUENCY RESPONSE: Block diagram representation of feedback amplifier, voltage series feedback, voltage shunt feedback differential amplifiers, frequency response compensating network, frequency response of internally compensative op-amp and non compensating op-amp. High frequency op-amp equivalent circuit, open loop gain V/s frequency, closed loop frequency response, circuit stability, slew rate.

UNIT-III
OP-AMP APPLICATION: DC, AC amplifiers, peaking amplifier, summing, scaling, averaging and instrumentation amplifier, differential input output amplifier, voltage to current converter, current to voltage converter, very high input impedance circuit, integration and differential circuit, wave shaping circuit, active filters, oscillators

UNIT-IV
SPECIALIZED LINER IC APPLICATIONS: 555 timer IC (monostable & astable operation) & its applications , Universal active filter, PLL, power amplifier, 8038 IC.

NOTE

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. R.A. Gayakwaed , OP-amps and Linear Integrated circuits .
2. K.R.Botkar , Integrated circuits.

B.TECH Vth SEMESTER
MICRO-ELECTRONICS
(ECE-309E)

L	T	P			
4	1	-	Theory	:	100
			Sessional	:	50
			Time	:	3Hrs

UNIT-I:
Crystal Growth: MGS, EGS, Czochralspi crystal Puller, Silicon shaping, Wafer Preparation.
Oxidation: Thermal Oxidation Kinetics, Oxidation Techniques, Oxide Properties, Oxidation induced defects. Thin film deposition techniques: Epitaxy, VDE, CVD, PECVD, MOCVD, PVD, Sputtering , MBE and epitaxial layer evaluations.

UNIT-II:
LithoGraphy, Photolithography, E-beam lithography, X-ray Lithography, reactive Plasma Etching, Plasma Properties, Feature Size control and anisotropic etching, Plasma etching techniques and equipment.

UNIT-III:
Diffusion : A Qualitative view of atomic diffusion in Solids, diffusion mechanisms, Fick's one dimensional diffusion equation, constant source and limited source diffusion, Diffusion of Grp3 and 5 impurities in Silicon Impurity Sources, diffusion apparatus, Characterization of diffused layers.
Ion Implantation: Introduction, Range Theory, Implantation Equipment Annealing.

UNIT-IV:
Isolation Techniques, Bipolar IC fabrication Process Sequence, N-MOS IC fabrication Process Sequence.
C-MOS IC fabrication Process Sequence .Assembly & Packaging: Package Types, design considerations, Package fabrication technologies, Future trends reference to MEMS packaging.

NOTE:
The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. S.M.Sze, VLSI Technology, Mc Graw Hill.
2. S.K.Ghandhi, VLSI Fabrication Principles.

B.TECH Vth SEMESTER
MICROPROCESSORS & INTERFACING
(ECE-311E)

L	T	P			
4	1	-	Theory	:	100
			Sessional	:	50
			Time	:	3Hrs

UNIT-I:
INTRODUCTION : Evolution of microprocessors, technological trends in microprocessor development. The Intel family tree. CISC Versus RISC. Applications of Microprocessors.
8086 CPU ARCHITECTURE : 8086 Block diagram; description of data registers, address registers; pointer and index registers, PSW, Queue, BIU and EU. 8086 Pin diagram descriptions. Generating 8086 CLK and reset signals using 8284. WAIT state generation. Microprocessor BUS types and buffering techniques, 8086 minimum mode and maximum mode CPU module.

UNIT-II:
8086 INSTRUCTION SET : Instruction formats, addressing modes, Data transfer instructions, string instructions, logical instructions, arithmetic instructions, transfer of control instructions; process control instructions; Assembler directives.
8086 PROGRAMMING TECHNIQUES : Writing assembly Language programs for logical processing, arithmetic processing, timing delays; loops, data conversions. Writing procedures; Data tables, modular programming. Macros.

UNIT-III:
MAIN MEMORY SYSTEM DESIGN : Memory devices, 8086 CPU Read/Write timing diagrams in minimum mode and maximum mode. Address decoding techniques. Interfacing SRAMS; ROMS/PROMS. Interfacing and refreshing DRAMS. DRAM Controller – TMS4500.

UNIT-IV:
BASIC I/O INTERFACE : Parallel and Serial I/O Port design and address decoding. Memory mapped I/O Vs Isolated I/O Intel's 8255 and 8251- description and interfacing with 8086. ADCs and DACs, - types, operation and interfacing with 8086. Interfacing Keyboards, alphanumeric displays, multiplexed displays, and high power devices with 8086.
INTERRRUPTS AND DMA : Interrupt driven I/O. 8086 Interrupt mechanism; interrupt types and interrupt vector table. Intel's 8259. DMA operation. Intel's 8237. Microcomputer video displays.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. D.V.Hall , Microprocessors and Interfacing , McGraw Hill 2nd ed.
2. J Uffenbeck , The 8086/8088 family , (PHI).
3. Liu,Gibson , Microcomputer Systems – The 8086/8088 family, (2nd Ed-PHI).

B.TECH Vth SEMESTER
LINEAR INTEGRATED CIRCUITS (Pr.)
(ECE-313E)

L	T	P			
-	-	3	Exam	:	25
			Sessional	:	50
			Time	:	3Hrs

1. To study OP-AMP as adder and sub tractor circuits(IC-741).
2. To study clipping circuits using OP-AMP(IC-741).
3. To study clamping circuits using OP-AMP(IC-741).
4. To study OP-AMP as Schmitt trigger(IC-741).
5. To study an instrumentation amplifier using OP-AMP(IC-741).
6. Study of current to voltage and voltage to current converter using OP-AMP(IC-741).
7. To study Astable multivibrator circuit using timer IC-555.
8. To study monostable multivibrator circuit using timer IC-555.
9. To study Voltage Controlled Oscillator using timer IC-555.
10. To study Frequency divider using IC-555.
11. To design 2nd order low pass butterworth filter.
12. To design 2nd order high pass butterworth filter.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope

B.TECH Vth SEMESTER
MICROPROCESSORS (Pr.)
(ECE-315E)

L	T	P			
-	-	3	Exam	:	25
			Sessional	:	50
			Time	:	3Hrs

Before starting with the experiments, teacher should make the students conversant with the following essential theoretical concepts.

A. i) Programming Model of Intel's 8086.
ii) Addressing Modes of Intel's 8086.
iii) Instruction formats of Intel's 8086

B. Instruction set of Intel's 8086.
C. Assembler , and Debugger.

LIST OF EXPERIMENTS:

I a) Familiarization with 8086 Trainer Kit.
b) Familiarization with Digital I/O, ADC and DAC Cards.
c) Familiarization with Turbo Assembler and Debugger S/Ws.

II Write a program to arrange block of data in
i) ascending and (ii) descending order.

III Write a program to find out any power of a number such that $Z = X^N$.
Where N is programmable and X is unsigned number.

IV Write a program to generate.
i) Sine Waveform (ii) Ramp Waveform (iii) Triangular Waveform Using DAC Card.

V Write a program to measure frequency/Time period of the following functions.
(i) Sine Waveform (ii) Square Waveform (iii) Triangular Waveform
using ADC Card.

VI Write a program to increase, decrease the speed of a stepper motor and reverse its direction of rotation using stepper motor controller card.

VII write a programmable delay routine to cause a minimum delay = 2MS and a maximum delay = 20 minutes in the increments of 2 MS

VIII a) Use DOS interrupt to read keyboard string/character.
b) Use BIOS interrupt to send a string/character to printer.

IX Write a program to :
i) Create disk file.
ii) Open, write to and close- a disk file.
iii) Open, read from and close a disk file.
iv) Reading data stamp of a file using BIOS interrupt.

X i) Erasing UVPROMs and EEPROMs
ii) Reprogramming PROMs using computer compatible EPROM Programmer.

XI Studying and Using 8086 In-Circuit Emulator.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope of syllabus.

B.Tech. (Common for all branches 5th/6th Semesters)
FUNDAMENTALS OF MANAGEMENT
HUT-302E

L	T
3	1

Theory : 100 Marks
Sessionals : 50 Marks
Total : 150 Marks
Time : 3 hours

UNIT-I **Financial Management**

Introduction of Financial Management, Objectives of Financial Decisions, Status and duties of Financial Executives. Financial Planning – Tools of financial planning. Management of working capital, Factors affecting requirements of working capital. Capital structure decisions. Features of appropriate capital structure. Sources of finance.

UNIT-II **Personnel Management**

Personnel Management – Meaning, Nature and Importance; Functions of Personnel Management – (a) Managerial Functions and (b) Operative functions. Job Analysis: Meaning and Importance; Process of Job Analysis; Job Description and Job specification. Human Resource Development-Meaning and concept.

UNIT-III **Production Management**

Production Management : Definition and Objectives
Plant location: Ideal plant location. Factors affecting plant location.
Plant Layout : Ideal plant layout, factors affecting plant layout.
Work Measurement : Meaning, Objectives and Essentials of work Measurement.
Production Control : Meaning and importance of production control and steps involved in production control.

UNIT-IV **Marketing Management**

Nature, scope and importance of marketing management. Modern Marketing concepts. Role of marketing in economic development. Marketing Mix. Marketing Information System. Meaning, nature and scope of International Marketing.

NOTE :

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. Business Environment – Francis Charurilam (Himalaya Publishing House).
2. Management – Harold, Koontz and Cyrilo' Donell (Mc Graw Hill)
3. Principles of Personnel Management – Edwin B. Flippo (Mc Graw Hill)
4. Personnel Management and Industrial Relations – D.C. Sharma and R.C. Sharma) (SJ Publications, Meerut)
5. Basic Marketing – Cundiff and Still (PHI, India)
6. Marketing Management – S.A. Sherlekar (Himalaya Publishing House Bombay)
7. Principles and Practice of Management – L.M. Prasad
8. Financial Management – I.M. Pandey (Vikas Publishing House, New Delhi)
9. International Marketing – Vorn terpestre and Ravi Sasathy.
10. Production Management – E.S. Buffa & W. H. Tausart, Richand D. Irwin, Homewood, Illionis.
11. Personnel Management – C.B. Mamoria, (Himalaya Publishing House)

B.TECH VI SEMESTER
CONTROL SYSTEM ENGINEERING
(ECE-302E)

L	T	P
4	1	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT-I :
INTRODUCTION: The control system-open loop & closed loop, servomechanism, stepper motor.
MATHEMATICAL MODELS OF PHYSICAL SYSTEMS: Differential equation of physical systems, transfer function, block diagram algebra, signal flow-graphs , Mason's formula & its application.
FEEDBACK CHARACTERISTICS OF CONTROL SYSTEMS: Feedback and non-feedback systems, Effects of feedback on sensitivity (to parameter variations), stability, overall gain etc.

UNIT-II:
TIME RESPONSE ANALYSIS: Standard test signals, time response of first order and second order systems, steady-state errors and error constants, design specification of second-order-systems.
STABILITY:The concept of stability ,necessary conditions for stability, Hurwitz stability criterion, Routh stability criterion, Relative stability analysis.
THE ROOT LOCUS TECHNIQUE:The Root locus concept, construction /development of root loci for various systems, stability considerations.

UNIT-III:
FREQUENCY RESPONSE & STABILITY ANALYSIS: Correlation between time and frequency response, Polar Plots, Nyquist plots, Bode Plots, Nyquist stability criterion, Gain margin & Phase margin, relative stability using Nyquist Criterion, frequency response specifications.

UNIT-IV:
COMPENSATION OF CONTROL SYSTEMS: Necessity of compensation, Phase lag compensation, phase lead compensation , phase lag lead compensation, feedback compensation .
STATE VARIABLE ANALYSIS : Concept of state,state variable and state model, state models for linear continuous time systems, diagonalization solution of state equations, concept of controllability and observability.

NOTE :

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

TEXT BOOK:
1. Control System Engg : I.J.Nagrath & M.Gopal; New Age India.

Reference Books:

1. Automatic Control Systems : B.C.Kuo; PHI.
2. Modern Control Engg : K.Ogata; PHI.
3. Control Systems: Principles & Designing : Madan Gopal; TMH.

B.TECH V1th SEMESTER
VHDL AND DIGITAL DESIGN
(ECE-304E)

L	T	P		
3	1	-	Theory :	100
			Sessional :	50
			Time :	3Hrs

UNIT I:
INTRODUCTION: History. Why use VHDL ? Hardware design construction, design levels, HDLs Hardware simulation and synthesis. Using VHDL for design synthesis, terminology.
PROGRAMMABLE LOGIC DEVICES :Why use programmable logic ? What is a programmable logic device ? Block diagram, macrocell structures and characteristics of PLDs and CPLDs. Architecture and features of FPGAs. Future direction of programmable logic.

UNIT II:
BEHAVIORAL MODELING:Entity declaration, architecture body, process statement, variable assignment, signal assignment. Wait, If, Case, Null, Loop, Exit, Next and Assertion statements. Inertial and transport delays, Simulation deltas, Signal drivers.
DATA FLOW AND STRUCTURAL MODELLING:Concurrent signal assignment, sequential signal assignment, Multiple drivers, conditional signal assignment, selected signal assignment, block statements, concurrent assertion statement, component declaration, component instantiation.

UNIT III:
GENERICS AND CONFIGURATIONS :Genericcs, Why configurations ?, default configurations, component configurations. Genericcs in configuration. Generic value specification in architecture, block configurations, architecture configurations.
SUBPROGRAMS AND PACKAGES :Subprograms – functions, procedures, declarations. Package declarations, package body, use clause, predefinal package standard. Design libraries, design file.

UNIT IV:
ADVANCED TOPICS :Generate Statements, Aliases, Qualified expressions, Type conversions, Guarded signals, User defined attributes, Predefined attributes., VHDL synthesis.

NOTE:
The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. D. Perry , VHDL, 3rd Ed.- TMH.
2. J.Bhasker, A.VHDL- Primer, PHI.
3. Skahil, VHDL for Programmable logic- 2nd Ed – Wiley.

B.TECH V1 SEMESTER
DIGITAL SIGNAL PROCESSING
(ECE- 306E)

L	T	P
3	2	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT – I:
DISCRETE TRANSFORMS: Z- transform and its properties, Inversion of Z-transform, One sided Z-transform and solution of differential equations. Analysis of LTI systems in Z-domain, causality, stability, schur-cohn stability test; relationship between Z-transform and Fourier transform. Frequency selective filters; all pass filters, minimum-phase, maximum-phase and mixed-phase systems.
Frequency domain sampling and DFT; properties of DFT, Linear filtering using DFT, Frequency analysis of signals using DFT, radix 2, radix-4, goertzel algorithm, Chirp Z-transform, applications of FFT algorithm, computation of DFT of real sequences. Quantization effects in computation of DFT.

UNIT – II:
IMPLEMENTATION OF DISCRETE TIME SYSTEMS: Direct form, cascade form, frequency sampling and lattice structures for FIR systems. Direct forms, transposed form, cascade form parallel form. Lattice and lattice ladder structures for IIR systems. State space structures Quantization of filter co-efficient structures for all pass filters.

UNIT – III:
DESIGN OF FIR FILTERS: Characteristics of practical frequency selective filters. Filters design specifications peak pass band ripple, minimum stop band attenuation. Four types of FIR filters Design of FIR filters using windows. Kaiser window method comparison of design methods for FIR filters Gibbs phenomenon, design of FIR filters by frequency sampling method, design of optimum equiripple FIR filters, alternation theorem.

UNIT – IV:
DESIGN OF IIR FILTERS: Design of IIR filters from analog filters, Design by approximation of derivatives, Impulse invariance method bilinear transformation method characteristics of Butterworth, Chebyshev, and Elliptical analog filters and design of IIR filters, Frequency transformation, least square methods, design of IIR filters in frequency domain.

NOTE:
The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. John G. Proakis, Digital Signal Processing, PHI
2. S. K. Mitra, Digital Signal Processing , TMH
3. Rabiner and Gold, Digital Signal Processing, PHI
4. Salivahan, Digital Signal Processing , TMH
5. Digital Signal Processing: Alon V. Oppenhelm;PHI

B. TECH. VI SEMESTER
DIGITAL COMMUNICATION
(ECE-308E)

L	T	P
3	1	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT – I:
PULSE MODULATION: sampling process, PAM and TDM; aperture effect. PPM noise in PPM, channel Bandwidth, Recovery of PAM and PPM signals Quantization process, quantization noise, PCM, μ Law and A- law compressors. Encoding, Noise in PCM, DM, delta sigma modulator, DPCM, ADM.

UNIT – II:
BASE BAND PULSE TRANSMISSION: Matched filter and its properties average probability of symbol error in binary enclosed PCM receiver, Intersymbol interference, Nyquist criterion for distortionless base band binary transmission, ideal Nyquist channel raised cosine spectrum, correlative level coding Duo binary signalling, tapped delay line equalization, adaptive equalization, LMS algorithm, Eye pattern.

UNIT – III:
DIGITAL PASS BAND TRANSMISSION: Pass band transmission model; gram Schmidt orthogonalization procedure, geometric Interpretation of signals, Response of bank of correlaters to noise input, detection of known signal in noise, Hierarchy of digital modulation techniques, BPSK, DPSK, DEPSK, QPSK, systems; ASK, FSK, QASK, Many FSK, MSK, Many QAM, Signal space diagram and spectra of the above systems, effect of intersymbol interference, bit symbol error probabilities, synchronization.

UNIT – IV:
SPREAD SPECTRUM MODULATION: Pseudonoise sequence, A notion of spread spectrum, direct sequence spread spectrum with coherent BPSK, signal space dimensionality & processing gain, probability of error, frequency spread spectrum, CDM.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. John G. Proakis, Digital Communication, PHI
2. Taub & Schilling, Principles of Communication, TMH
3. Simon Haykin, Communication systems, John Wiley & Sons

B.TECH V1 SEMESTER
COMPUTER COMMUNICATION NETWORKS
(ECE-310E)

L	T	P			
3	1	-	Theory	:	100
			Sessional	:	50
			Time	:	3Hrs

.

UNIT – I:
INTRODUCTION: Uses of Computer Networks, Network Hardware, Network Software, Reference models, Examples of Networks & Data communication Services, Network Standardization.
THE PHYSICAL LAYER: The Theoretical basis for Data communication, Transmission media, Wireless Communication, The Telephone System, Narrowband ISDN, Broadband ISDN and ATM, Cellular Radio, Communication Satellites.

UNIT – II:
THE DATA LINK LAYER: Data Link Layer Design issues, Error Detection & correction, Elementary Data Link protocols, Sliding Window Protocols, Protocol Specification & Verification, Example of Data Link Protocols.
THE MEDIUM ACCESS SUBLAYER: Aloha Protocols, LAN Protocols, IEEE Standards, Fiber optic Networks, Satellite Networks, Packet switching, radio Networks.

UNIT – III:
NETWORK LAYER: Design issues, routing algorithms, congestion control Algorithms, internetworking.
TRANSPORT & SESSION LAYER: Protocol design issues, connection Management, remote procedure calls.

UNIT – IV:
PRESENTATION LAYER: Design issues, abstract Syntax notation, data compression technique, cryptograph.
APPLICATION LAYER: Design issues, file transfer, access and management, electronic mail, virtual terminals, applications and examples.

Suggested Books:

1. Tanenbaum A.S, Computer Networks, PHI.
2. Forouzan B.A, Data Communications and Networking, Tata-Mc-Graw Hill.
3. Stallings W, Data and Computer Communications, PHI.
4. Ahuja V, Design and Analysis of Computer Communication, McGraw Hill.
5. Bee K.C.S, Local Area Networks, NCC Pub.
6. Davies D. W. Barber, Computer Networks and their Protocols, John Wiley.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

B.TECH VI SEMESTER
DIGITAL COMMUNICATION PRACTICAL
(ECE-312E)

L	T	P
-	-	3

Sessional	:	50
Viva	:	25
Time	:	3Hrs

LIST OF EXPERIMENTS:

1. To Study PSK
2. To Study FSK
3. To Study IF Amplifier
4. To Study Balanced Modulator & Demodulator
5. To Study PCM
6. Setting up a Fiber Optic Analog Link
7. Setting up a Fiber Optic Digital Link
8. Losses in Optical Fiber
9. Measurement of Numerical Aperture
10. Time Division multiplexing of signals.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope

B.TECH V1th SEMESTER
ELECTRONICS DESIGN PRACTICAL
(ECE-314E)

L	T	P			
-	-	3	Exam	:	25
			Sessional	:	50
			Time	:	3Hrs

LIST OF EXPERIMENTS:

1. Design a single stage R C Coupled amplifier and plot its gain frequency response.
2. Design a two stage R C Coupled amplifier and plot its gain frequency response.
3. Design a R C Phase shift oscillator using IC 741.
4. Design a wein bridge oscillator.
5. Design a square wave generator using IC 555.
6. Design a 4 : 1 multiplexer and 1 : 4 demultiplexer using logic gates.
7. Design a parallel parity bit generator using ICs.
8. Design a digital to analog converter using ICs.
9. Design a digital frequency meter (0-999HZ) using IC 555 for monoshot, IC-7404,7408,7490,7447.
10. Design a controller such that LEDs glow in pairs sequentially using IC 7490 and LEDs.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope

B.TECH V1th SEMESTER
VHDL PRACTICAL
(ECE-316E)

L	T	P			
-	-	3	Exam	:	50
			Sessional	:	50
			Time	:	3Hrs

LIST OF EXPERIMENTS:

1. Write a VHDL Program to implement a 3 :8 decoder.
2. Write a VHDL Program to implement a 8:1 multiplexer using behavioral modeling.
3. Write a VHDL Program to implement a 1 :8 demultiplexer using behavioral modeling.
4. Write a VHDL Program to implement 4 bit addition/subtraction.
5. Write a VHDL Program to implement 4 bit comparator.
6. Write a VHDL Program to generate Mod- 10 up counter.
7. Write a VHDL Program to generate the 1010 sequence detector. The overlapping patterns are allowed.
8. Write a program to perform serial to parallel transfer of 4 bit binary number.
9. Write a program to perform parallel to serial transfer of 4 bit binary number.
10. Write a program to design a 2 bit ALU containing 4 arithmetic & 4 logic operations.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope